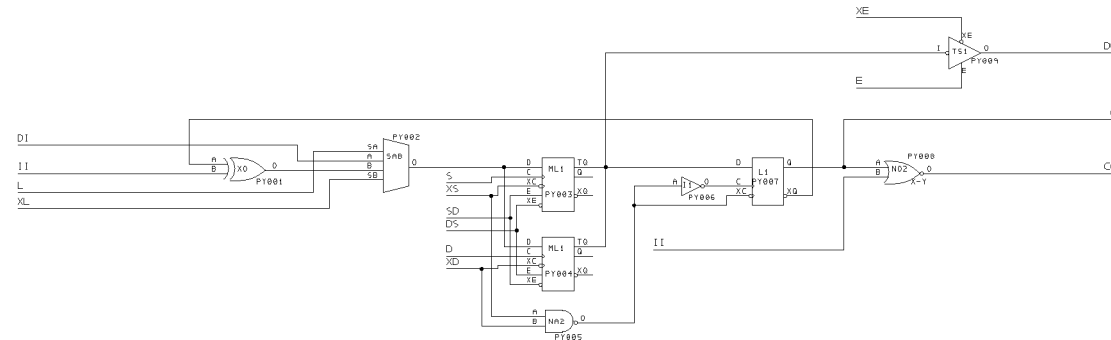
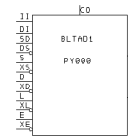
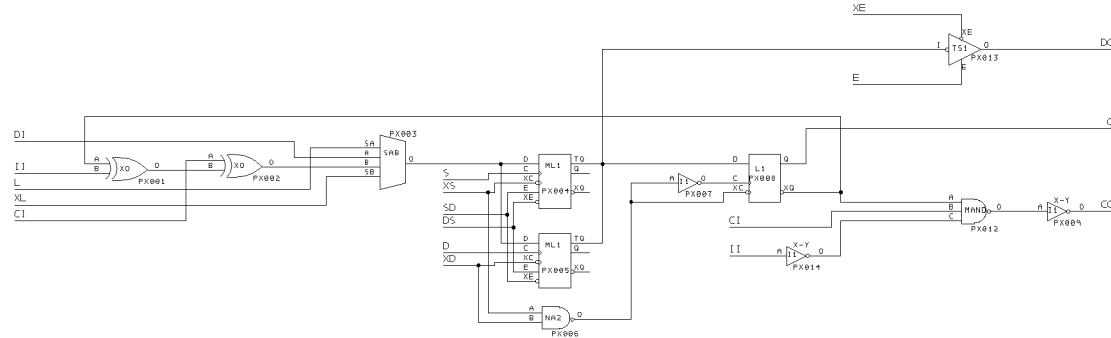
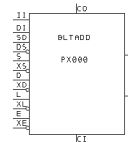
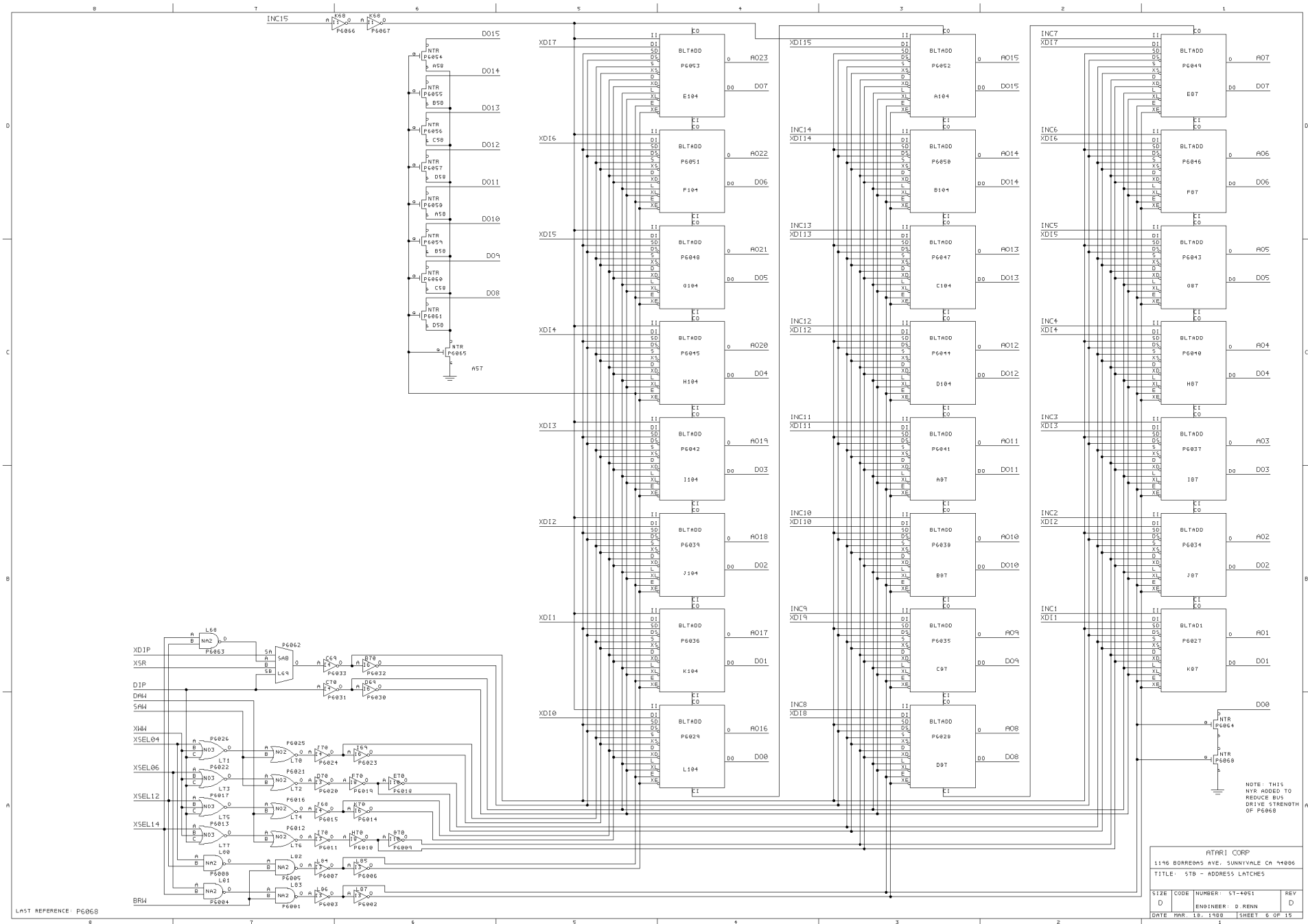
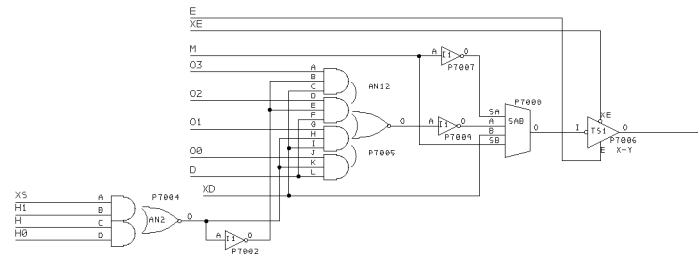


NOTE: THIS DESIGN WAS MODIFIED TO BUFFER THE DO OUTPUT AND INVERT THE O OUTPUT. THE DO OUTPUT WENT FROM A TO A T51. THIS PREVENTS DATA BUS LOADING FROM AFFECTING THE OPERATION OF THE BLT CELL, AND SPEED UP THE READ CYCLE TIMING. THE O OUTPUT WAS INVERTED SO THAT A SUBSEQUENT INVERTER ON THE SAME LINE ON PAGE B COULD ALSO BE REMOVED. THIS WILL SAVE 1,5X23 GATES, AND WILL SPEED UP THE ADDRESS BUS RESPONSE BY A FEW NANoseconds.

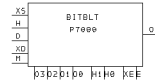
NOTE #2: THIS DESIGN WAS AGAIN MODIFIED TO COMPENSATE FOR THE INVERSION OF THE INC AND DI INPUTS. THE INVERTERS ADDED ABOVE WERE REMOVED, WHICH FIXED THE DI INPUT. AND THE X0 WAS CONVERTED TO AN XN FOR THE INC INPUT. HOWEVER, THE XN OF THE OUTPUT OF AN XN WITH A THIRD NUMBER IS THE SAME AS THE X0 TO THE OUTPUT OF AN X0 AND THE THIRD NUMBER. THEREFORE, ALL OF THE XN'S HAVE BEEN REMOVED.







- NOTE: BITBLT HAS HAD A LOT OF CHANGES IN IT.
1. THE H INPUT HAS HAD AN INVERTER REMOVED IN ORDER TO COMPENSATE FOR INVERTED DATA BEING STORED IN THE RAM.
 2. THE SA AND SB INPUTS OF THE S40 HAVE BEEN SWAPPED TO COMPENSATE FOR INVERTED DATA COMING IN ON THE H INPUT.
 3. THE OUTPUT TO WAS REPLACED WITH A TS1 CELL. THE AN12 COULD NOT DRIVE THE HEAVILY LOADED DATA BUS THROUGH BOTH THE S40 AND THE T9.
 4. AS A RESULT OF (3.), AN INVERTER WAS ADDED TO THE OUTPUT OF THE AN12 TO RESTORE THE CORRECT POLARITY TO THE OUTPUT SIGNAL.
 5. ALSO AS A RESULT OF (3.), THE S INPUT OF THE S40 HAS BEEN INVERTED BY TAKING IT FROM THE OUTPUT OF THE INVERTER P7002.



ATARI CORP			
1146 BORREONS AVE. SUNNYVALE CA 94086			
TITLE: BITBLT CELL DEFINITION			
SIZE	CODE	NUMBER: ST-4051	REV
D		ENGINEER: D. RENN	D
DATE	MAR 18, 1988	SHEET 7 OF 15	

