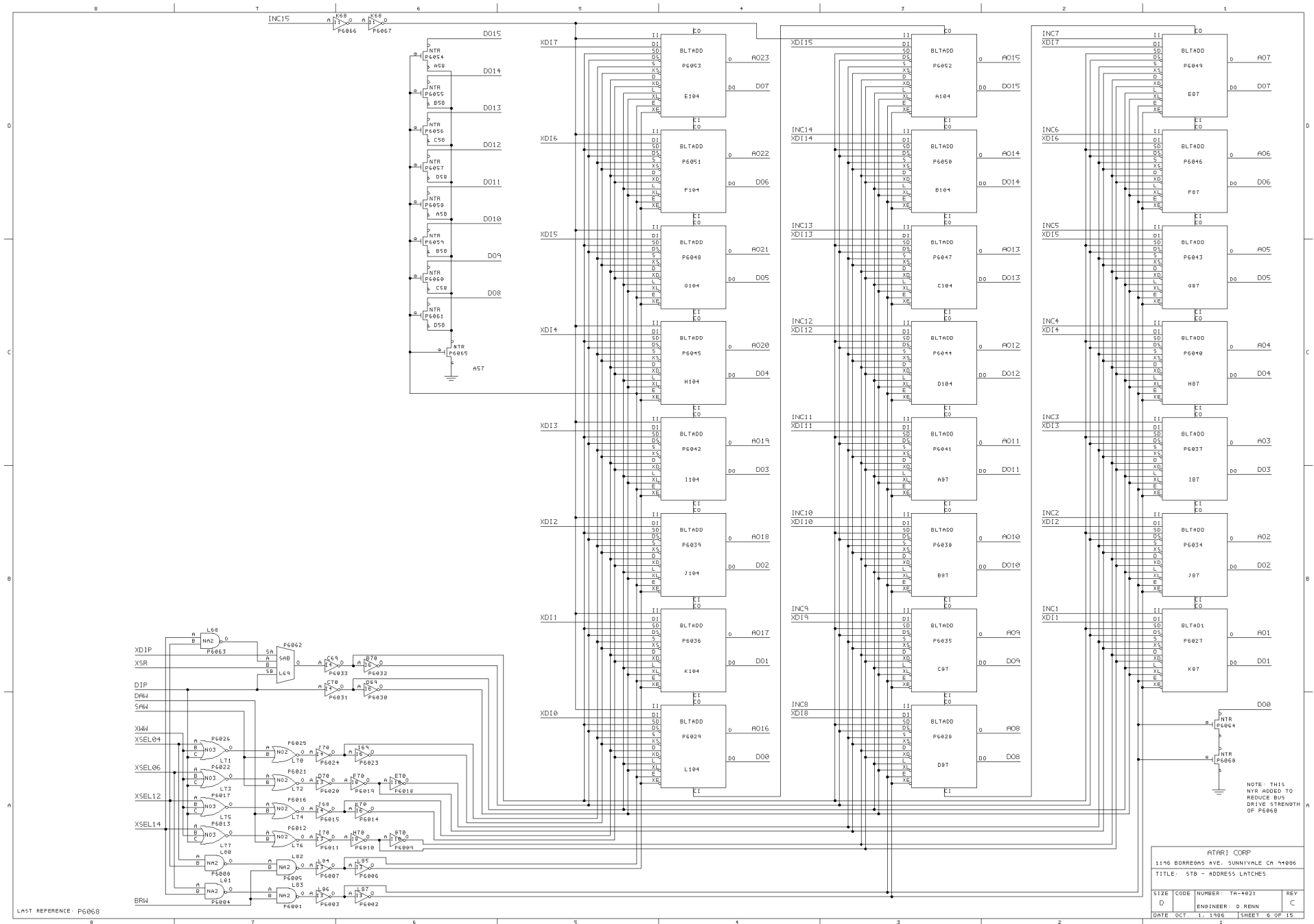
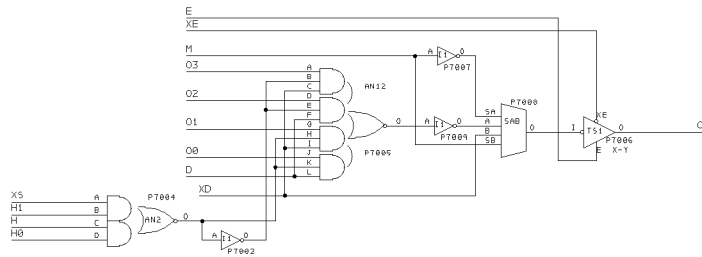


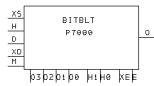
NOTE #2: THIS DESIGN WAS AGAIN MODIFIED TO COMPENSATE FOR THE INVERSION OF THE INC AND DI INPUTS. THE INVERTERS LOGGED ABOVE WERE REMOVED, WHICH FIRED THE DI INPUT, AND THE X0 WAS CONVERTED TO AN XN FOR THE INC INPUT. HOWEVER, THE XN OF THE OUTPUT OF AN XN WITH A THIRD NUMBER IS THE SAME AS THE X0 TO THE OUTPUT OF AN X0 AND THE THIRD NUMBER. THEREFORE, ALL OF THE XN'S HAVE BEEN REMOVED.

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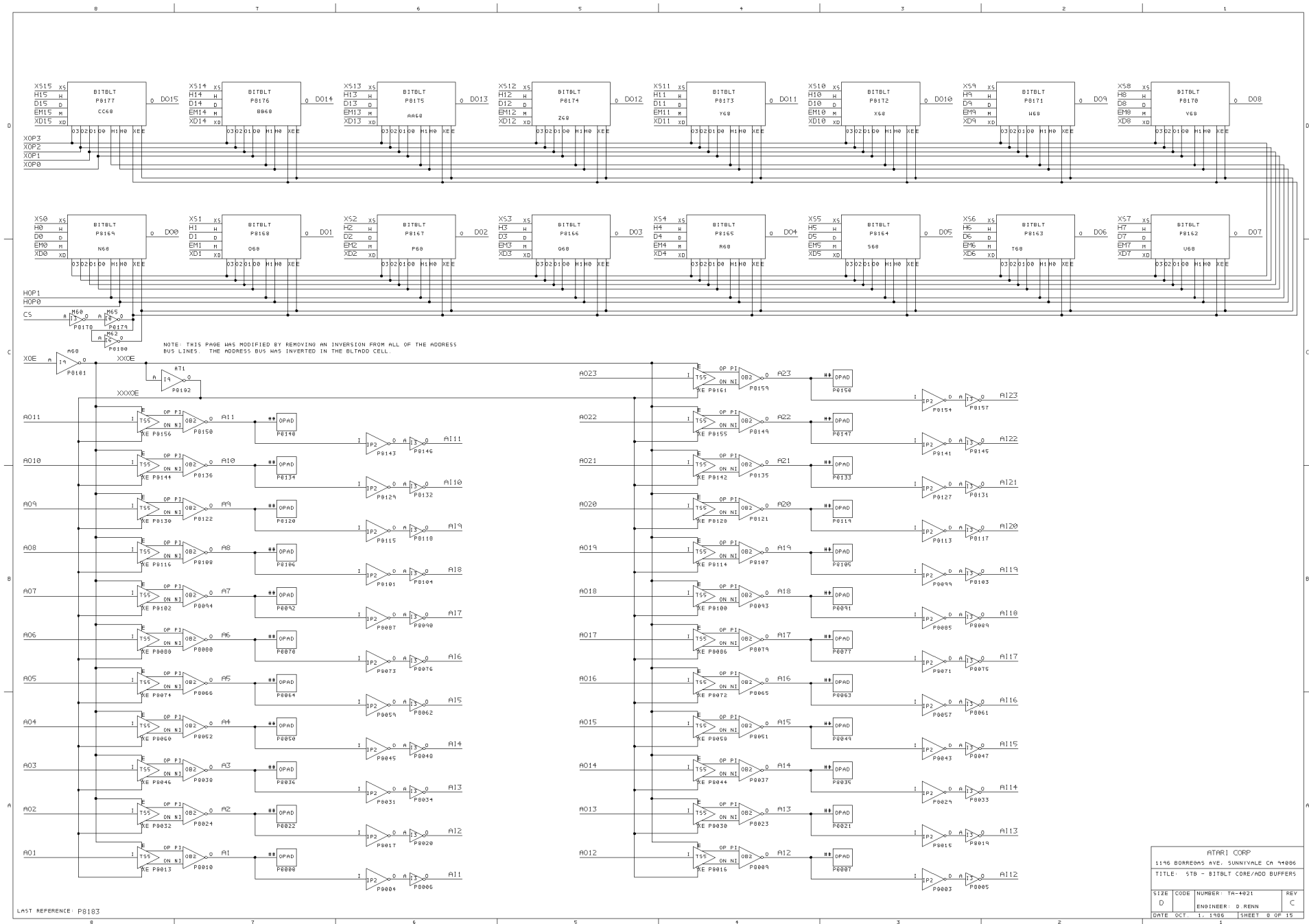


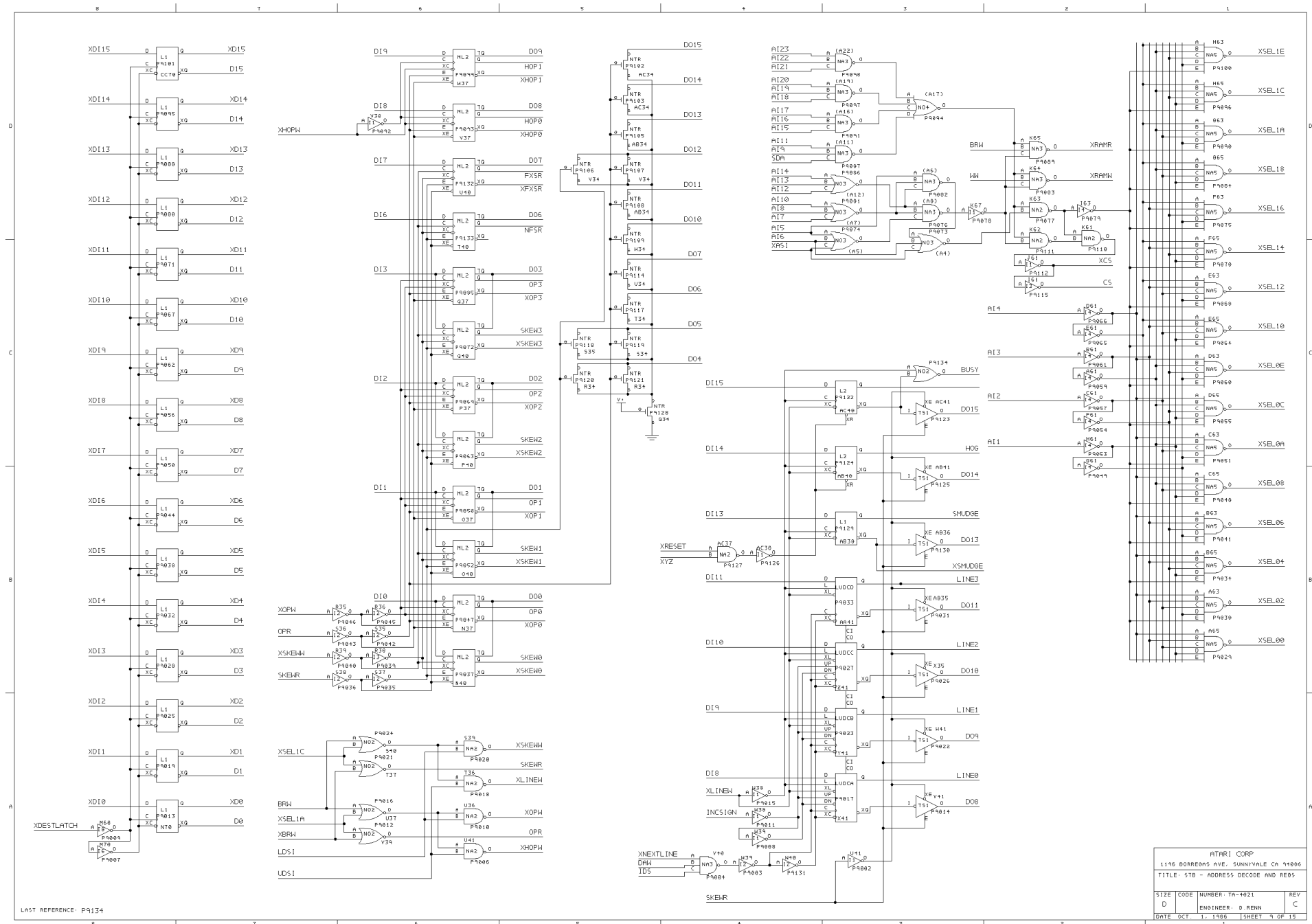


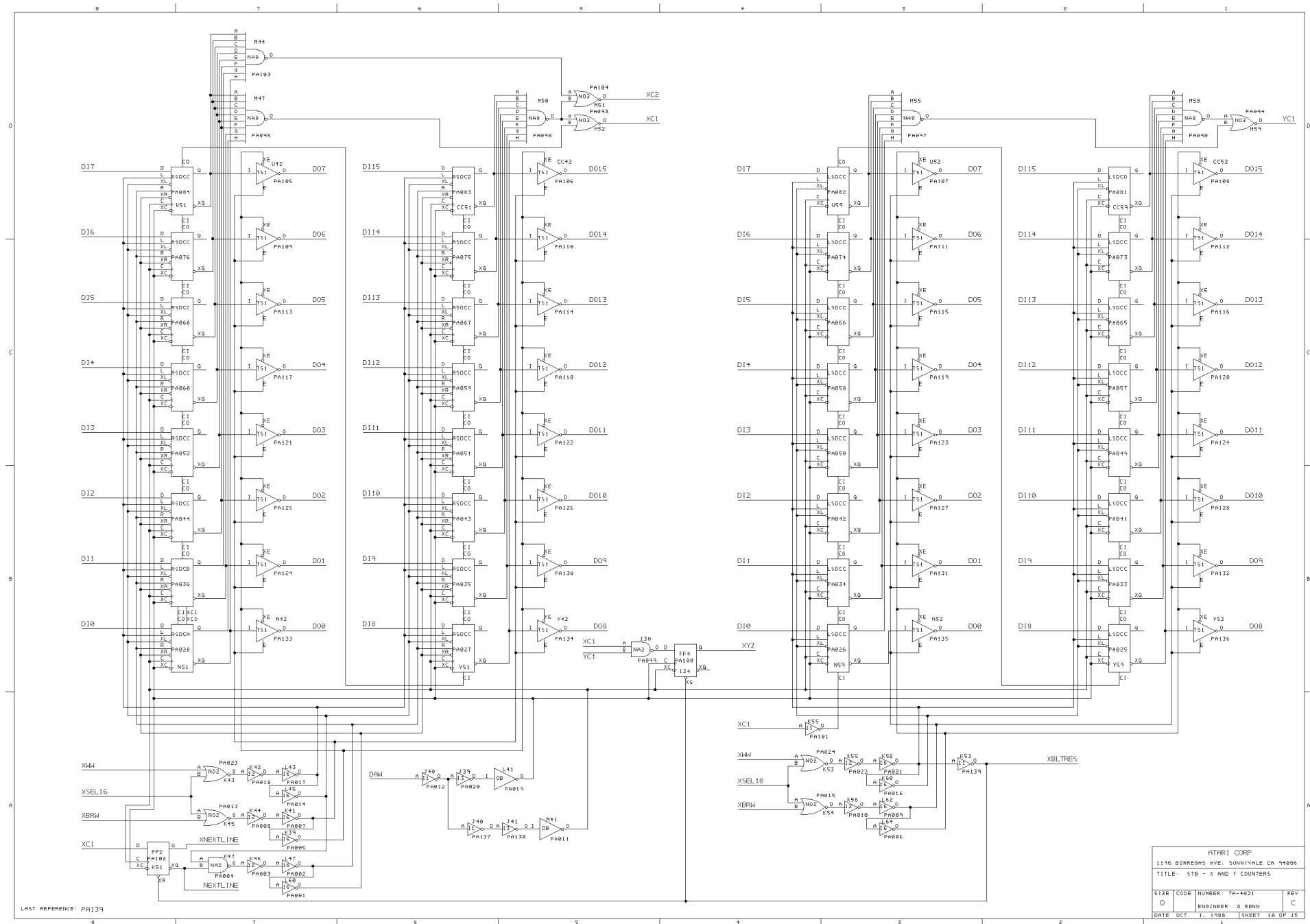
- NOTE: BITBLT HAS HAD A LOT OF CHANGES IN IT.
1. THE A INPUT HAS HAD AN INVERTER REMOVED IN ORDER TO COMPENSATE FOR INVERTED DATA BEING STORED IN THE RAM.
 2. THE SA AND SB INPUTS OF THE SAB HAVE BEEN SWAPPED TO COMPENSATE FOR INVERTED DATA COMING IN ON THE H INPUT.
 3. THE OUTPUT TO WAS REPLACED WITH A TS1 CELL. THE AN12 COULD NOT DRIVE THE HEAVILY LOADED DATA BUS THROUGH BOTH THE SAB AND THE T9.
 4. AS A RESULT OF (3.), AN INVERTER WAS ADDED TO THE OUTPUT OF THE AN12 TO RESTORE THE CORRECT POLARITY TO THE OUTPUT SIGNAL.
 5. ALSO AS A RESULT OF (3.), THE B INPUT OF THE SAB HAS BEEN INVERTED BY TAKING IT FROM THE OUTPUT OF THE INVERTER P7003.

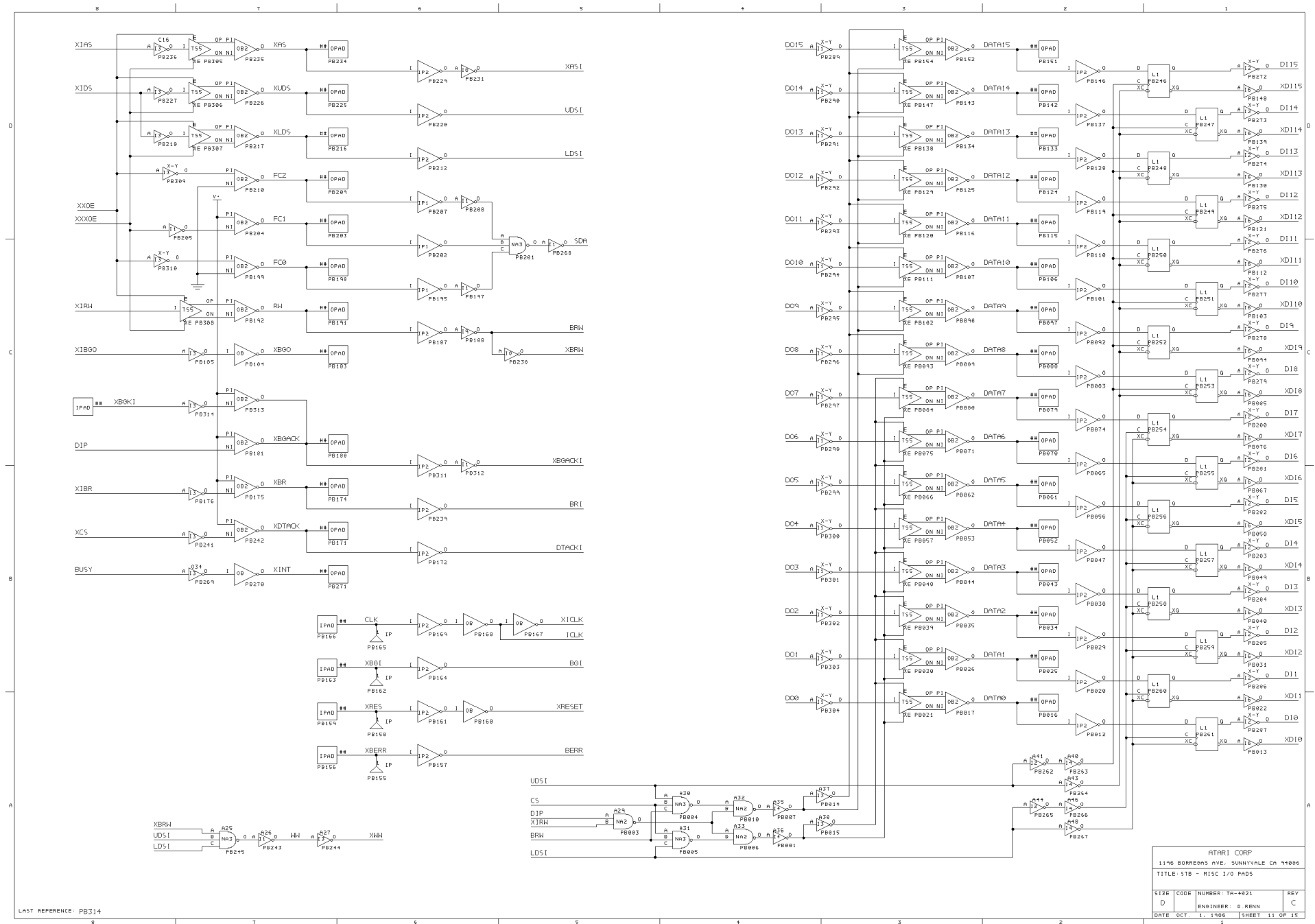


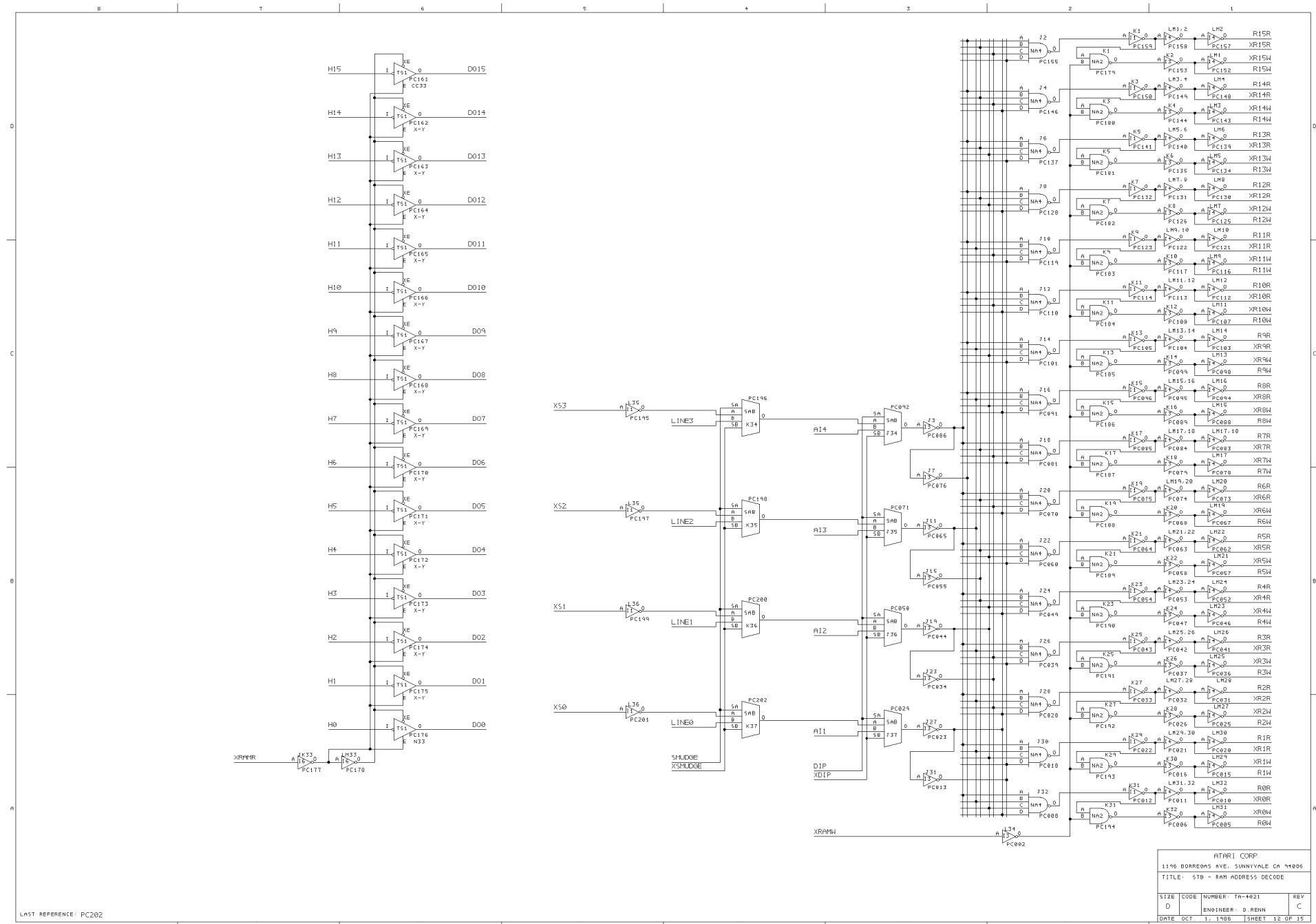
ATARI CORP			
1146 BORREONS AVE. SUNNYVALE CA 94086			
TITLE: BITBLT CELL DEFINITION			
SIZE	CODE	NUMBER: TA-4021	REV
D		ENGINEER: D. RENN	C
DATE	OCT. 1, 1986	SHEET 7 OF 15	















LAST REFERENCE: PE128

ATARI CORP			
1146 BORREONS AVE, SUNNYVALE, CA 94086			
TITLE: 5TB - HALFTONE RAM			
SIZE	CODE	NUMBER: TA-4021	REV
D		ENGINEER: D. RENN	C
DATE OCT. 1, 1986		SHEET 14 OF 15	

