

PCB Layout Guide for USB2504

Introduction

This application note provides information on designing a printed circuit board (PCB) for SMSC USB2504 USB Hub Controller. The PCB requires only two layers of copper.

Two Layer PCB

A successful PCB with only two copper layers for the USB2504 decreases the total cost of a finished USB Hub compared to a four-layer design. However, the design of the PCB will require more care to maintain controlled USB impedance and to provide good supply and ground paths. This application note addresses several of these issues. The self-powered hub evaluation board EVB-USB2504-CRB is used as an example for this application note. The schematic for this board is shown in the appendix.

PCB Constraints

- Material: FR-4
- Copper thickness: 1.0 to 2.0 ounces
- Dielectric Thickness: 47 mils
- Form-factor: 3.42" x 2.68"

PCB Considerations

- Control differential impedance on USB traces (90 Ohms)
- Isolate USB traces from other circuitry and signals
- Shield on up-stream connector should be tied to shield on down-stream connectors with a low impedance, wide and isolated trace, preferably along the periphery of the design.
- Provide adequate low impedance supply connection to down-stream ports' VBUS
- Keep bulk capacitors for down-stream port's VBUS power close to connectors
- Isolate crystal and oscillator
- Isolate RBIAS resistor and keep traces short
- Bypass capacitors placed on top side - no components on bottom side for reduced assembly cost

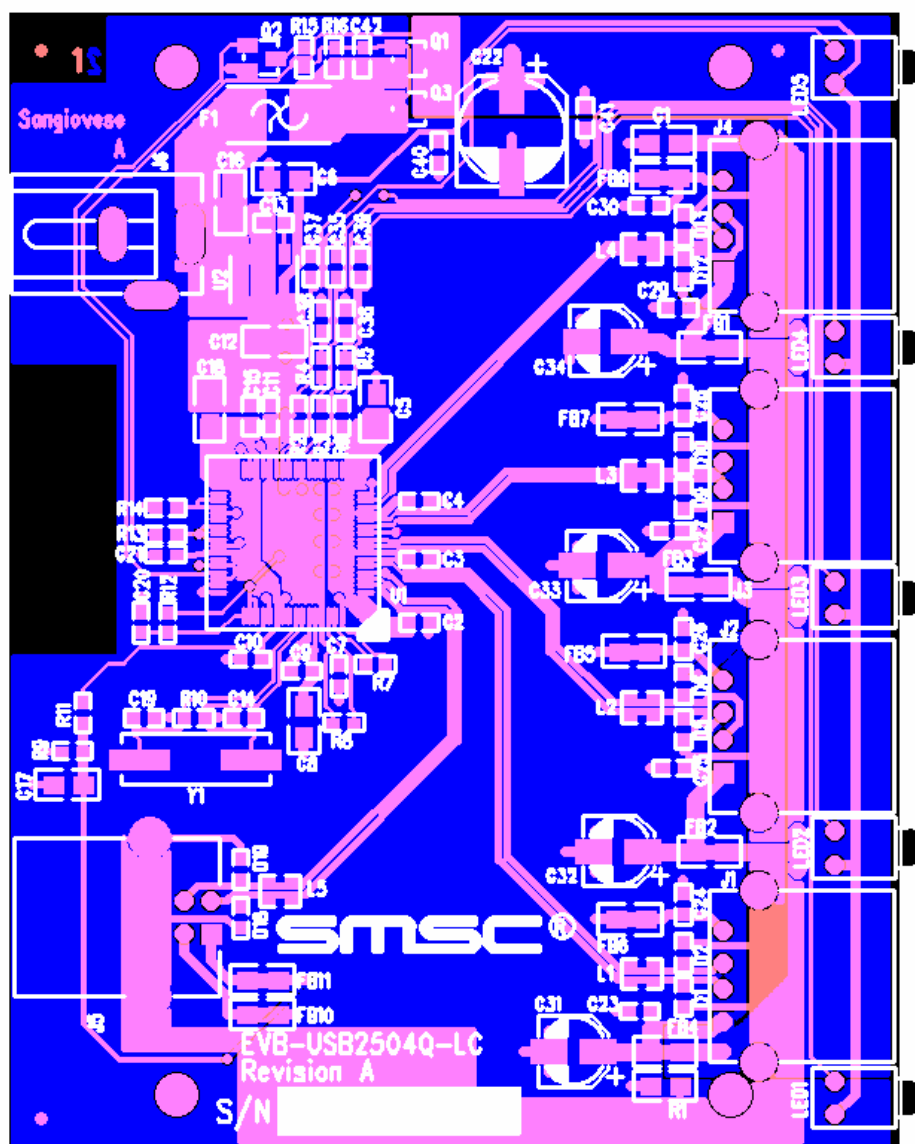


Figure 1 Overall view with three layers shown: Top silk-screen (white), top copper layer (red) and bottom copper layer (blue).

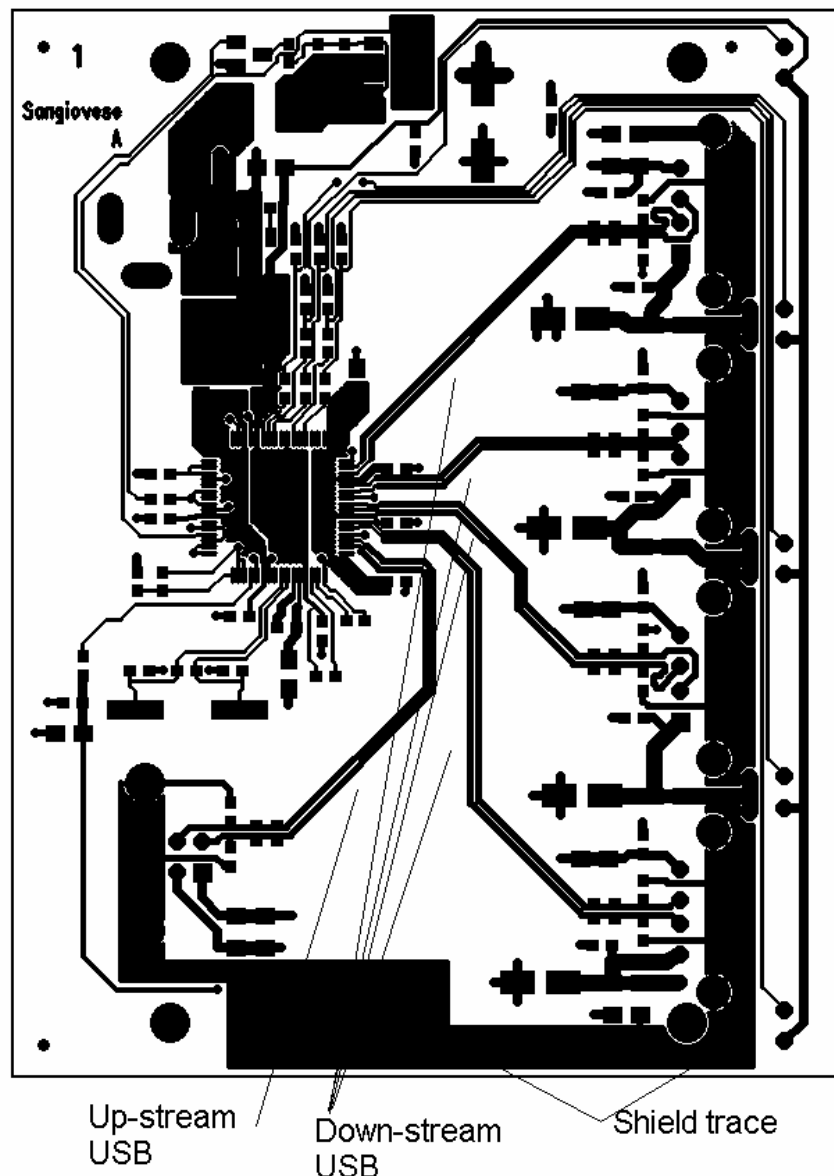


Figure 2 Top layer copper: USB traces and shield.

Controlled Impedance for USB Traces

The USB2.0 specification requires that USB DP/DM traces maintain nominally 90 Ohms differential impedance. In this design the USB DP/DM traces are 18 mils wide with 7 mils spacing. A continuous ground plane is required directly beneath the DP/DM traces and extending at least 5 times the spacing width ($5 \times 7 = 35$ mils) to either side of DP and DM.

- Maintain close to 90 Ohms differential impedance. For different dielectric thickness, copper thickness or board stack-up, trace width and spacing needs to be recalculated.
- Maintain symmetry between DP and DM in regards to shape. Trace lengths should be matched.
- Keep unrelated signal traces, supplies and components away from DP/DM traces. A good rule of thumb is 5 times the trace width (or 35 mils) in this design. This minimizes coupling effects and impedance mismatch along the trace.

- Single ended impedance is not as critical as the differential impedance. A range from 45 to 80 ohms is acceptable.

In [Figure 3](#) the USB traces are 18 x 7 mils, but close to the pads of the USB2504 they are tapered down to 7 mils wide to access the pads of the USB2504. The discontinuity in the trace causes an impedance mismatch. It is important to keep the length of the discontinuity as short as possible to reduce its impact to the USB signal quality. The design rules for the PCB process and pad size requirements for efficient assembly has higher priority versus the ideal trace impedance.

Another example of a compromise is that the ideal clearance distance of 35 mils is not met near the chip as shown in [Figure 3 on page 4](#). Decoupling capacitors are placed as close to the chip as possible to keep series inductance low. Since the capacitors are mounted on the top side only one via in series with the capacitor is needed to connect to the ground plane on the bottom layer. Note that in this case the clearance is twice the spacing, (14 mils) near between the pads for the capacitor and DP/DM traces. The pad size is small relative to the overall trace length. Keeping this spacing as large as possible, and keeping the length of the violation as short as possible makes the negative effect on the impedance mismatch smaller.

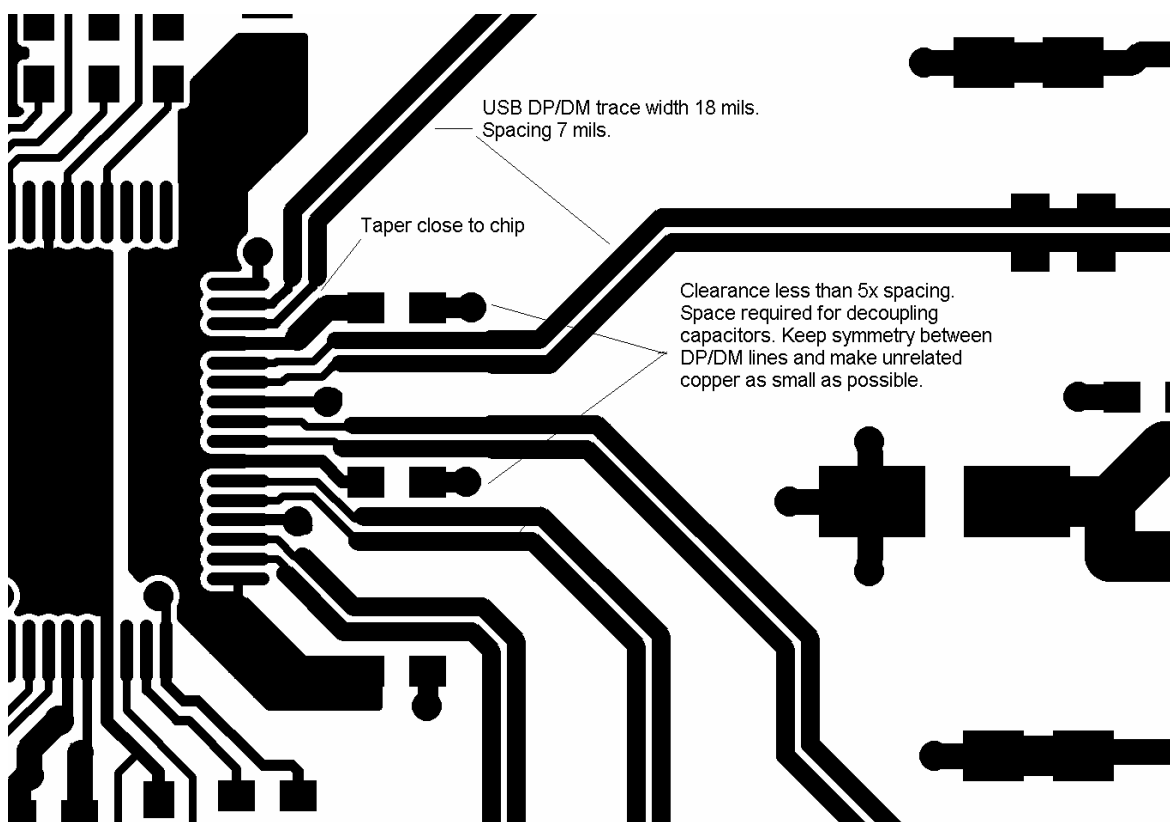


Figure 3 USB DP/DM traces to up-stream and down-stream ports (top copper layer).

Shield

For self-powered hubs with isolated main power supplies the shield on down-stream USB connectors is tied to the up-stream USB port shield. The shield is isolated from the signal ground. [Figure 2](#) shows the shield on the top layer and [Figure 4 on page 5](#) shows the shield on the bottom copper layer isolated from the signal ground. A wide trace on the periphery away from other signals should connect the down stream port's shield with the up-stream port's shield. This is important to minimize effects from ESD immunity events. If the main power supply is earth grounded for a self-powered hub, connect the shield as a separate trace to a single earth ground point near the entry point for the power supply on the board.

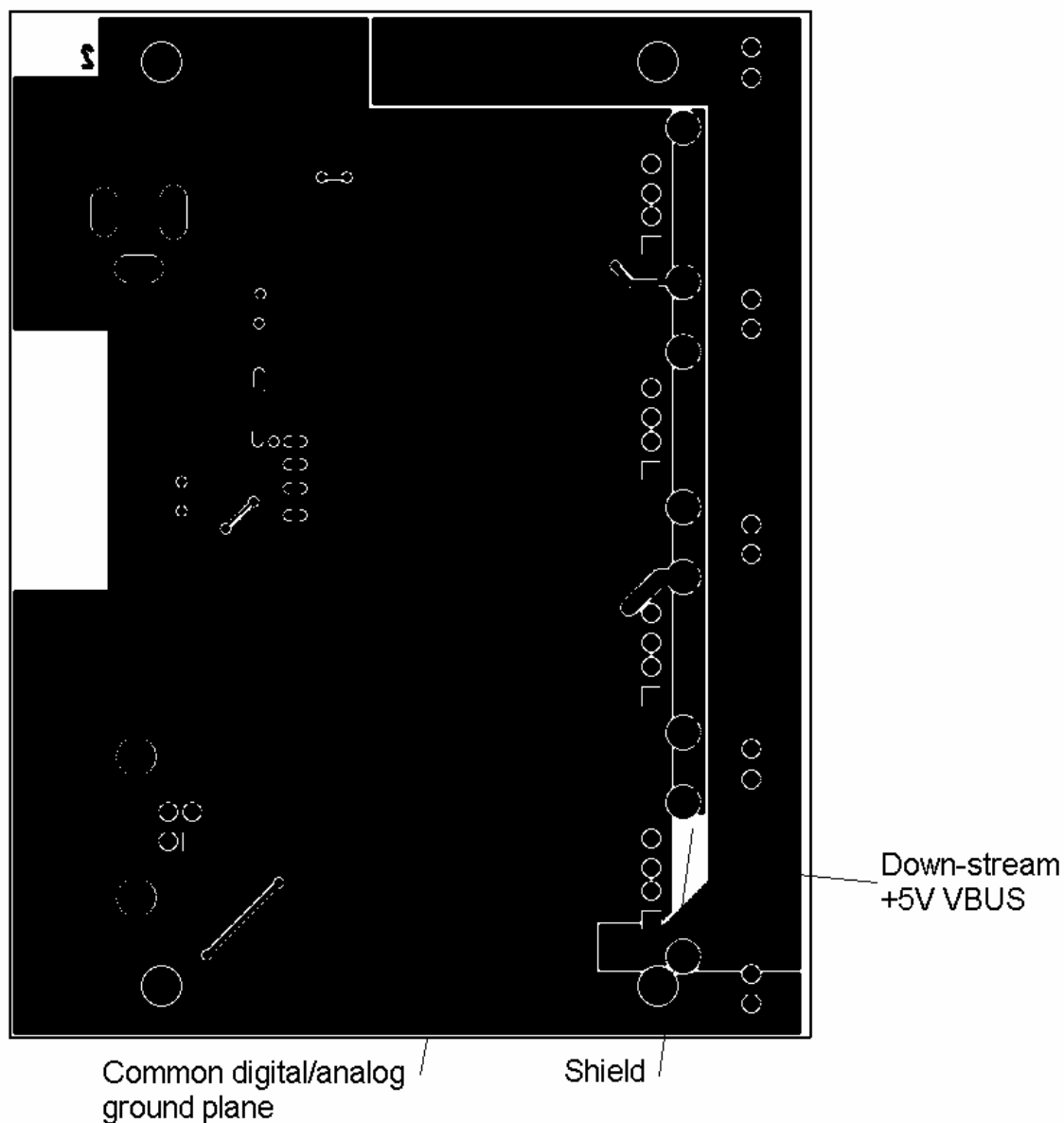


Figure 4 Shows bottom layer copper: common ground, shield and down-stream VBUS distribution.

VBUS Supply

Down-stream ports supply power to plugged-in devices. For self-powered hubs the maximum current per port is limited to 500mA. This design is self-powered with four down-stream ports that has a ganged over current protection device. The maximum current from the supply to the down-stream ports is 2A. It is carried on the wide +5V VBUS trace along the upper and right side of the design shown in [Figure 4 on page 5](#).

There are two USB-IF tests directly targeting board layout and circuit design that should be considered. The first test is the drop test, which measures the VBUS voltage under full load on all down-stream ports. This test requires that the voltage drop from the main supply is limited. Therefore traces carrying VBUS power must be wide and short to minimize the IR drop under full load. The second test is the droop test, which measures the effect when a device is first plugged in while all other ports are fully loaded. A 10uF capacitive load in parallel with a 50 Ohms resistive load emulates the device in this

test. The momentary droop in voltage on the loaded ports has to be minimized by minimizing charge sharing from one port to the other. Make supply and return paths wide and short, and consider using thicker copper on the PCB ($\geq 1.5\text{oz.}$), to lower instantaneous voltage drops. Fan out the supply traces from on board bulk capacitors to each down-stream port in such a way to minimize the impact of each port's effect on the other.

Crystal Oscillator

The crystal oscillator is sensitive to stray capacitances and noise from other signals. It can also disturb other signals and cause EMI noise. The load capacitors, crystal and parallel resistors should be placed close to each other. The ground connection for the load capacitors should be short and out of the way from return currents from USB, VBUS and digital logic power supply.

Figure 5 on page 6 shows the crystal circuit consisting of the crystal Y1, load capacitors C14 and C19 and parallel resistor R10. All four components are moved away from USB traces. The bottom side is solid ground under this circuit and no other traces are adjacent to the main X1 and X2 signals.

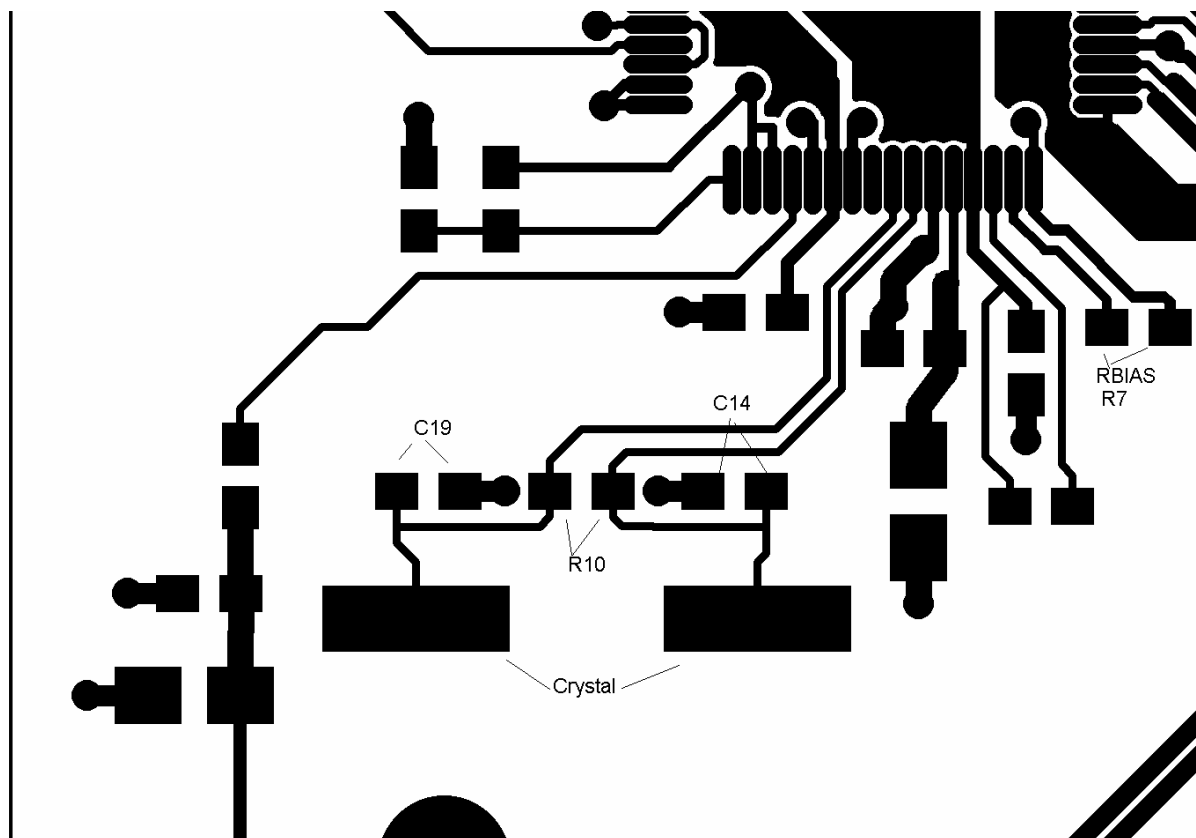


Figure 5 Detail of crystal, load capacitors C14, C19, parallel resistor R10 and RBIAS R7.

RBIAS

The RBIAS resistor provides the external reference for DC levels internal to the device. Any noise induced on the RBIAS traces directly impacts internal references and eye-diagram quality. The RBIAS resistor should be placed very close to RBIAS (pin 63) and the ground return should be short and direct to the corresponding VSS (pin 64) on the USB2504. Traces for RBIAS should be very short, direct, and 5 times the trace width away from any other traces if possible, especially the XTAL1 and XTAL2 crystal circuit traces. Figure 5 shows the RBIAS connection with the ground connection to pin 64.

Bypass Capacitors

This example has bypass capacitors for the HUB placed on the top side of the board as shown in [Figure 6](#) and [Figure 7](#) shows the same area with the top side copper traces. There is a tradeoff in cost by requiring two-pass assembly versus board space. In this example board space is dictated by the space required for USB connectors so there is space to put all components on one side allowing for single pass assembly. Bypass capacitors should be placed close to the supply pins of the USB2504 with short and wide traces. Critical capacitors are C8 for VDDA18 and C18 for VDD18. Capacitors may carry large currents that cause magnetic fields that will induce noise into nearby traces. Sensitive traces such as USB, crystal and RBIAS should be separated by at least 5 times the trace width from decoupling capacitors when possible.

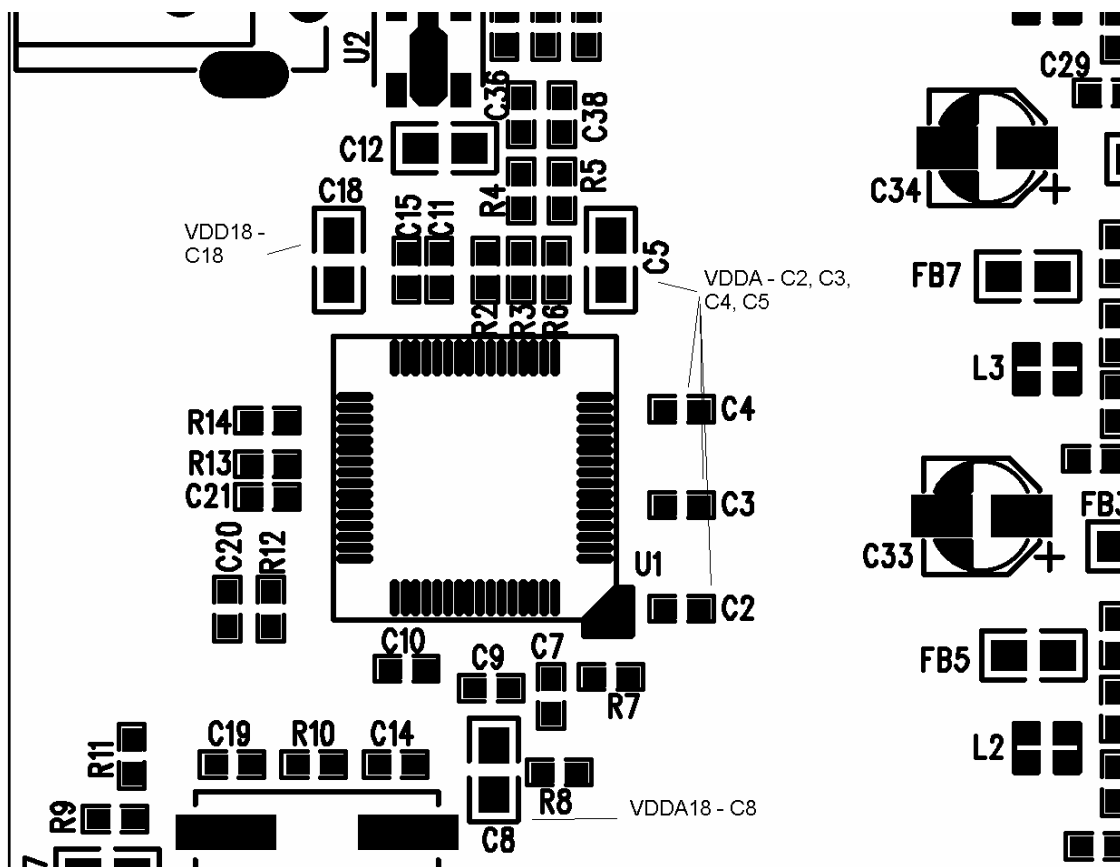


Figure 6 Detail of top side decoupling capacitors.

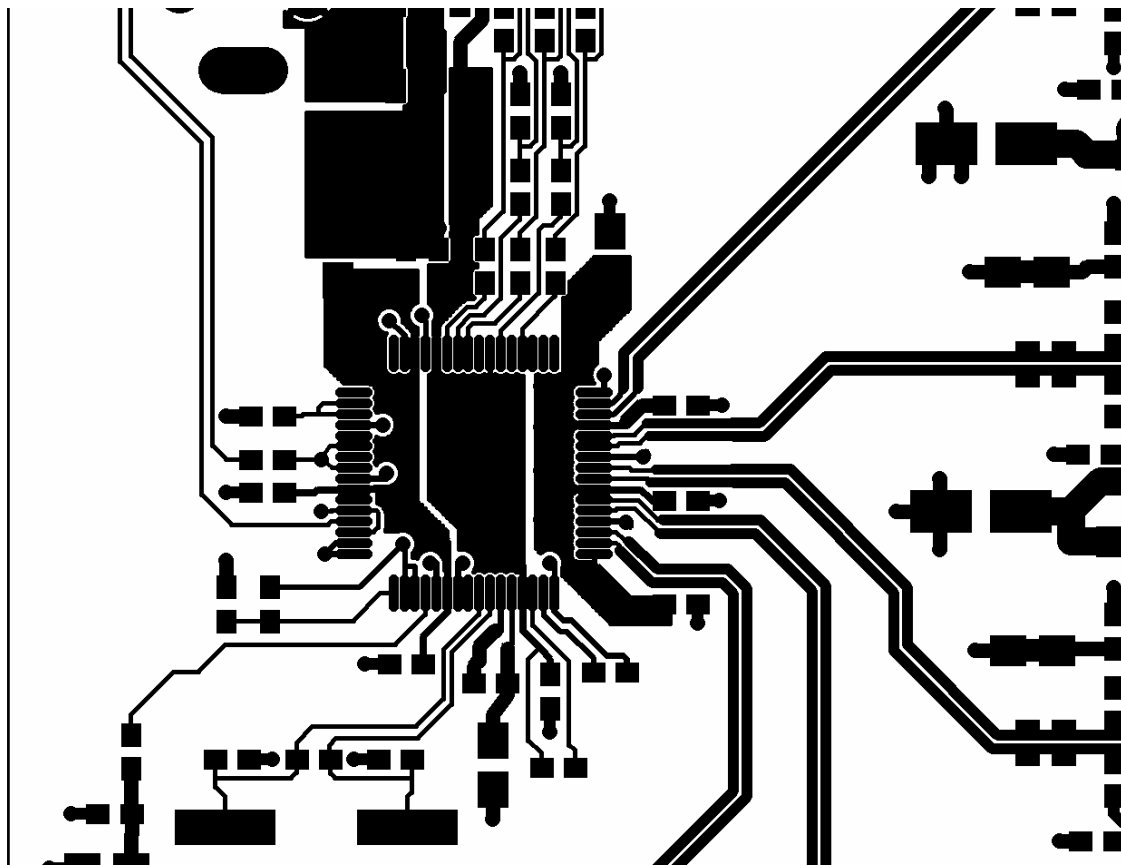


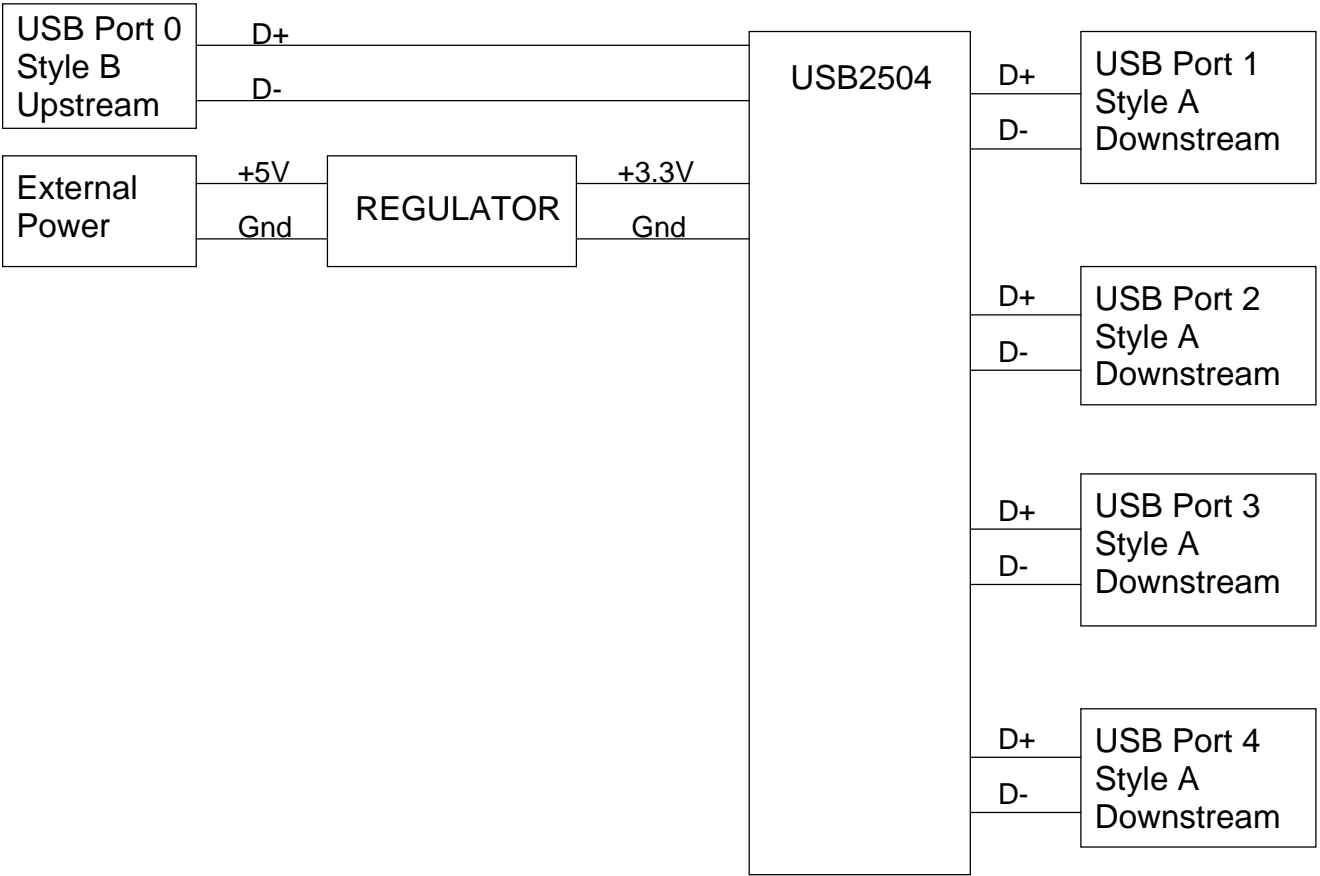
Figure 7 Top side traces fan-out from the USB2504.

Appendix: EVB-USB2504-CRB Schematic

See figures on following pages.

EVB-USB2504Q-LC

Evaluation Board for USB2504, 64-pin QFP, 2 Layers



Revision History			
Revision	Date	Revision Summary	Author
0.1-0.5	09/01/2004	Initial schematic	Edward Tatum
0.6	09/13/2004	Added title page, block diagram.	Carl Johnson
0.7	09/15/2004	Added caps to USB power pins, renumbered.	Carl Johnson
0.8	09/17/2004	Changed all 10uF caps to 4.7uF for cost reduction, added port-power control ckt, added EMI caps on LED lines, simplified the termination fo the EEPROM signals, changed the time constant of the reset ckt, standardized on 100K for pu and pd resistor values, removed FB9, standardized on 0.1uF caps for VDD bypass, changed VBUSDET ckt to improve ESD isolation, changed the USBPWR_GANG cap to 330uF to help pass droop test, removed the varistors on USB power and ground for all ports, identified the 47uF caps on ports 1-4 as DNP.	Carl Johnson
A	09/17/2004	Released	Carl Johnson
A1	10/13/2004	Change pick point of OCS_GANG, renumber LEDs, replaced obsolete regulator, changed values of VBUS_DET resistors.	Carl Johnson



80 Arkay Drive
Hauppauge, NY 11788
(631) 435-6000
FAX (631) 273-3123

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